

LICENSABLE
INTELLECTUAL
PROPERTY
FOR FPGA, ASIC OR
ASSP DESIGNS

1G

Ultra-Low Latency
1G Ethernet MAC
and PCS

ULTRA-LOW LATENCY, HIGH-SPEED, FLEXIBILITY AND SCALABILITY.

APPLICATIONS

- High Frequency Trading
- Smart NIC
- Low-Latency Switches
- Low-Latency Radio
- Test and Monitoring Equipment

The Ultra-Low Latency 1G Ethernet MAC and PCS is the industry leading solution for latency critical Ethernet applications. The core is designed using advanced design techniques leading to unmatched ultra-low gate count utilization and amazing latency performances.

It includes a rich set of standard and advanced features making it ideal for a large number of applications. The IP core can support full wire line speed with a 64-byte packet length. It also supports back-to-back or mixed length traffic, up to jumbo frame size, with no dropped packets.

GENERAL FEATURES

Compliant with the IEEE 802.3-2012 High Speed Ethernet Standard

Ethernet MAC supports 1GbE line rate with flexible feature set

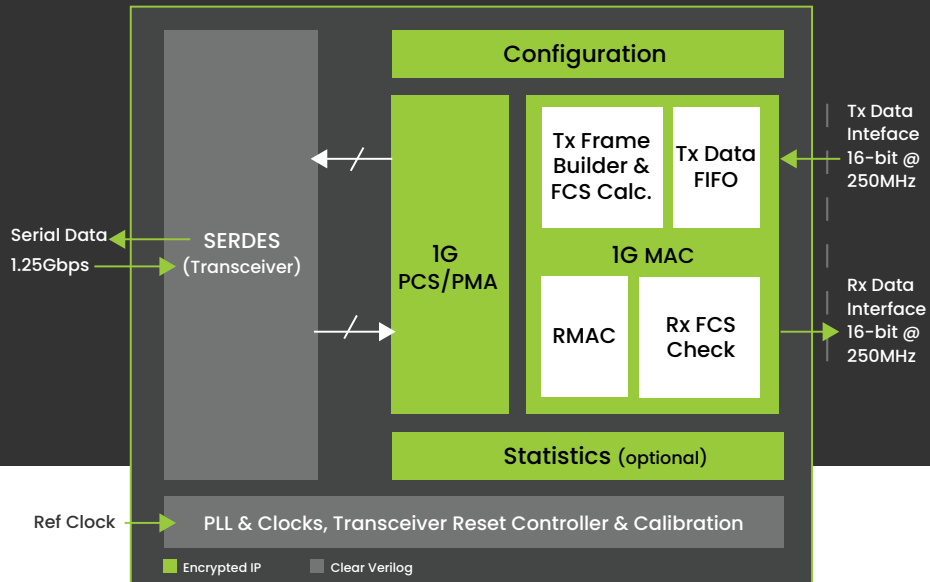
Soft PCS logic interfacing to standard serial transceiver at 1.25Gbps

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Contact us for a personalized evaluation and to discuss the best way to try our products.

HIGH-LEVEL BLOCK DIAGRAM



DELIVERABLES

- Datasheet & user guide
- Encrypted Verilog
- Constraints file
- Reference design
- Technical support
- Optional IP design customization

ORDERING INFORMATION

ENET-001G-L-01 (1G)

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MAC FEATURES

- Deficit idle counter (DIC) to maintain a 12-byte inter-packet gap (IPG) average
- Programmable IPG length (down to 1-byte)
- Programmable Maximum Receive Unit (MRU), Maximum Transmission Unit
- User facing logic interface 16-bit @ 250MHz
- Ethernet flow control and congestion management using pause frames with programmable quanta
- Programmable Tx minimum packet length with enable/disable padding option
- Programmable Rx minimum packet length
- Tx Frame Check Sequence (FCS) computation and insertion
- Programmable Tx FCS pass-through and corruption insertion modes
- Programmable keep/strip Rx FCS
- Programmable Rx FCS error detection and marking
- Programmable Tx and Rx path VLAN detection (Programmable TPID, stacked VLAN)
- Configurable statistics vector and collector on transmit and receive MAC data

PCS FEATURES

- Supports 1000BASE-X PHY based on 8B/10B encoding
- Running disparity compute
- Configurable statistics vector and collector on transmit and receive PCS

PERFORMANCES OVERVIEW EXAMPLE

Device Family ⁽¹⁾	Rate [Gbps]	Resources Utilization ⁽²⁾			Core clock [MHz]	Latency Measurements	Wire to Wire Round-Trip Latency ⁽³⁾
		LUTs	FFs	BRAM			
UltraScale +	1-Gbps	2.28k	4.14k	0	250	TxSoP to RxSoP	136ns
						TxSoP to RxSoF	64ns

(1) Other FPGA platforms supported

(2) Resources utilization includes statistics counters

(3) Latency: GTY Transceiver + PCS + MAC (Tx+Rx)